Note:

- Minimum 12 experiments should be conducted:
- All these experiments are to be simulated first either using MATLAB, COMSIM or any other simulation package and then to be realized in hardware

LIST OF EXPERIMENTS:

1. PCM Generation And Detection
2. Differential Pulse Code Modulation
3. Delta Modulation
4. Adaptive Delta Modulation
5. Time Division Multiplexing Of 2 Band Limited Signals
6. Frequency Shift Keying: Generation And Detection
7. Phase Shift Keying: Generation And Detection
8. Amplitude Shift Keying: Generation And Detection
9. DPSK :Generation And Detection
10. QPSK : Generation And Detection
11. OFDM: Generation And Detection
12. Spectrum Analyzer

Major Equipments required for Laboratories:

1. CROs: 20MHz
2. Function Generators: 2MHz
3. Spectrum Analyzer
4. Regulated Power Supplies: 0-30V
5. Analog and Digital Modulation and Demodulation Trainer Kits.
AIM:
To analyze a PCM system and interpret the modulated and demodulated waveforms for a sampling frequency of 4 KHz.

APPARATUS:
1. PCM modulator trainer
2. PCM Demodulator trainer
3. C.R.O (30MHz)
4. Patch chords.

INTRODUCTION

In Pulse code modulation (PCM) only certain discrete values are allowed for the modulating signals. The modulating signal is sampled, as in other forms of pulse modulation. But any sample falling within a specified range of values is assigned a discrete value. Each value is assigned a pattern of pulses and the signal transmitted by means of this code. The electronic circuit that produces the coded pulse train from the modulating waveform is termed a coder or encoder. A suitable decoder must be used at the receiver in order to extract the original information from the transmitted pulse train.

This PCM system consists of

PCM Modulator
1. Regulated power supply
2. Audio Frequency signal generator
3. Sample & Hold circuit
4. 8 Bit A/D Converter
5. 8 Bit Parallel-Serial Shift register
6. Clock generator/Timing circuit
7. DC source

2.3.2. PCM Demodulator
1. Regulated power supply
2. 8 Bit Serial-Parallel to shift register
3. 8 Bit D/A converter
4. Clock generator
5. Timing circuit
6. Passive low pass filter
7. Audio amplifiers
Regulated power supply (68M & 68D):
This consists of a bridge rectifier followed by capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of +5V and +12V @ 300Ma each to the on board circuits. These supplies have been internally connected to the circuits, so no external connections are required for operation.

Audio Frequency (AF) Signal generator (68M):
Sine wave signal of 200Hz is generated to use as a modulating (message or information) signal to be transmitted. This is an Op-Amp based Wein bridge Oscillators using IC TL084. IC TL084 is a FET input general purpose Operational Amplifier. Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

Clock generator/Timing circuit (68M & 68D):
A TTL compatible clock signal of 64 KHz and 4KHz frequency are provided on board to use as a clock to the various circuits in the system. This circuit is a astable multivibrator using 555 timer followed by a buffer and frequency dividers.

DC source (68M):
A 0 to +5V variable DC voltage is provided on board to use as a modulating signal instead of AF signal. This is useful to study step by operation of PCM modulation and demodulation. This is a simple circuit consisting of potentiometer and fixed power supply.

Low pass filters (68D):
This is a series of simple RC networks provided on board to smoothen the output of the D/A converter output (stair case signal). RC values are chosen such that the cutoff frequency would be at 200Hz
**Amplifiers (68D):**

This is an Op-amp (IC TL084) based non-inverting variable gain amplifiers provided on board to amplify the recovered message singles i.e. output of the Low pass filter to desired level. Amplitude control is provided in circuit to vary the gain of the amplifier between 0 and 3. AC/DC Switch facilitates to couple the input signal through capacitor or directly to the amplifier input.

**Sample & Hold circuit (AET-68M):**

This block (circuit) is a combination of buffer, level shifting network and sample & hold network. Op-amp IC TL084 is connected as buffer followed by non-inverting summer circuit. One of the inputs of summer is connected a voltage divider network and other being drawn as input. A dedicated sample & hold integrated circuit LF 398 is used as an active component followed by buffer. The LF198/LF298/LF398 is monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth.

Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of 1010(Ohm) allows high source impedance to be used without degrading accuracy.

P-channel junction FET’s are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μf hold capacitor. The JFET’s have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages. Logic inputs on the LF198 are fully differential with low current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from +5V to +18V supplies.

**8 Bit A/D Converter (AET-68M):**

This has been constructed with a popular 8 bit successive approximation A/D Converter IC ADC0808. The ADC0808, data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals. A dedicated 1MHz clock generator is provided in side this block. For complete specifications and operating conditions please refer the data sheet of ADC0808.
8 Bit Parallel-Serial Shift register (AET-68M):

A dedicated parallel in serial out shift register integrated circuit is used followed by a latch. The SN74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse.

Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function.

Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. For complete specifications and operating conditions please refer the data sheet of SN74LS166.

8 Bit Serial-Parallel Shift register (AET-68D):

A dedicated serial in parallel out shift register integrated circuit is used followed by a latch. The SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register.

Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all TTL products. For complete specifications and operating conditions please refer the data sheet of SN74LS164.

8 Bit D/A Converter (AET-68D):

This has been constructed with a popular 8 bit D/A converter IC DAC 0808. The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150ns while dissipating only 33mW with +5V supplies. No reference current (IREF) trimming is required for most applications since the full scale output current is typically +1 LSB of 255 IREF/256. Relative accuracies of better than +0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4μA provides 8-bit zero accuracy for IREF >= 2mA.

The power supply currents of the DAC0808 are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. For complete specifications and operating conditions please refer the data sheet of DAC0808.
**PCM Operation:**

The block diagram of the PCM system. The modulating signal is applied to sample & hold circuit. This applied signal will be super imposed by +2.5V DC so that the negative portion the modulating signal will clamped to positive, this process is needed, because input of the A/D Converter should be between 0 and +5V. After level shifting is done the signal will be passed to sample & hold circuit. Sample & hold circuit will sample the input signal during on period of the clock signal and will hold the sampled output till next pulse comes. Sampling rate is 4KHz in this system.

So input of the A/D Converter is a stable voltage of certain level in between 0 and +5V. A/D converter (encoder) will give a predetermined 8 bit code for the sampled input. This entire conversion process will be made at a fast rate as ADC0808 is operating at high frequency clock i.e. 1MHz. Coded output of the A/D converter is applied to input of the parallel in serial out register through a latch (741s373). This shift register is operating at 64KHz (sampling frequency is 4KHz, so to shift 8 bits from parallel to serial we need 64KHz). This output (PCM) is transmitted through a co-axial cable which represents a communication channel.

PCM signal from modulator (encoder) is applied to serial to parallel register. This shift register is also operating at 64KHz clock at which parallel to serial shift register is operating at PCM modulator (these both the clock signals should be in synchronized with each other in order to get proper decoded output). So the output of the serial to parallel register is a 8 bit code. This 8 bit code is applied to 8 bit D/A converter. Output of the D/A converter will be a staircase signaling between 0 and +5V. This stair case signal is applied a low pass filter. This low pass will smoothen the staircase signal so that we will get a recovered AF signal. We can use a voltage amplifier at the output of the low pass filter to amplify the recovered AF signal to desired voltage level.

**PROCEDURE:**

1. Connect the modulator trainer to the mains and switch on the power supply.
2. Observe the output of the AF generator using CRO, it should be a sine wave of 200Hz frequency with 3Vpp amplitude.
3. Verify the output of the DC source with multimeter/scope, output should vary from 0 to +5V.
4. Observe the output of the clock generator using CRO, they should be 64KHz and 4KHz frequency of square wave with 5Vpp amplitude.
5. The clock signals are internally connected the circuit so no external connections are required
6. Connect the demodulator trainer to the mains and switch on the power supply.
7. Observe the output of the clock generator using CRO, it should be 64KHz square wave with 5Vpp amplitude.
PCM Operation (with DC input):
Modulation:
8. Set DC source to some value say 4.4V with the help of multimeter and connect it to the A/D converter input and observe the output LED’s
9. Note down the digital code i.e. output of the A/D converter and compare with the theoretical value.

Theoretical value can be obtained by: \[ \frac{A_{input \ voltage}}{1LSB \ Value} = X_{(10)} = Y_{(2)} \]

Where
\[ 1LSB \ Value = \frac{V_{ref}}{2^n} \]
Since \( V_{ref} = 5V \) and \( n=8 \)
\[ 1LSB \ Value = \frac{5}{2^8} = 0.01953 \]

Example:
\[ A/D \ Input \ Voltage = 4.4V \]
\[ 225.28_{(10)} \]
\[ 11100001_{(2)} \]

So digital output is 11100001
10. Keep CRO in dual mode. Connect one channel to 4KHz signal (one which is connected to the Shift register) and another channel to the PCM output.
11. Observe the PCM output with respect to 4 Khz signal and sketch the waveforms.
   Compare them with the given waveforms
   Note: From this waveform you can observe the LSB bit enters the output first.

Demodulation
12. Connect PCM signal to the demodulators(S-P shift register) from the PCM modulator (AET-68M) with the help of coaxial cable.
13. Connect clock signal (64KHz) from the transmitter (AET-68M) to the receiver (AET-68D) using co axial cable.
14. Connect transmitter clock to the timing circuit.
15. Observe and note down the S-P shift register output data and compare it with transmitted data(i.e. output A/D converter at transmitter).You will notice that the output of the S-P shift register is following the A/D converter output in the modulator.
16. Observe D/A converter output (Demodulated output) using multimeter /scope and compare it with the original signal and you can observe that there is no loss in information in process of conversion and transmission.

Sample work sheet:
1. Modulating signal : 4.4 V
2. A/D Output (theoretical) : 1110 0001(2)
3. A/D Output (practical) : 1110 0001(2)
4. S-P Output : 1110 0001(2)
5. D/A Converter output : 4.4 V
PCM Operation (with AC input):

Modulation:
17. Connect AC signal of 2Vpp amplitude to Sample & Hold circuit.
18. Keep the CRO in dual mode. Connect one channel to the AF signal and another channel to the Sample & Hold output. Observe and sketch the sample & hold output.
19. Connect the Sample and Hold output to the A/D converter and observe the PCM output using Storage oscilloscope.
20. Observe PCM output by varying AF signal voltage.

Demodulation:
21. Connect PCM signal to the demodulator input (AET-68D) (S-P shift register) from the PCM modulator (AET-68M) with the help of coaxial cable (supplied with the trainer).
22. Connect clock signal (64 KHz) from the transmitter (AET-68M) to the receiver (AET-68D) using coaxial cable.
23. Connect transmitter clock to the timing circuit.
24. Keep CRO in dual mode. Connect CH1 input to the sample and hold output (AET-68M) and CH2 input to the D/A converter output (AET-68D)
25. Observe and sketch the D/A output.
26. Connect D/A output to the LPF input.
27. Observe the output of the LPF/Amplifier and compare it with the original modulating signal (AET-68M).
28. From above observation you can verify that there is no loss in information (modulating signal) in conversion and transmission process.
29. Disconnect clock from transmitter (AET-68M) and connect to local oscillator (i.e., Clock generator output from AET-68D) with remaining setup as it is.
Observe D/A output and compare it with the previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

Note: You can take modulating signals from external sources. Maximum amplitude should not exceed 4V incase of DC and 3 Vpp incase AC (AF) signals.
EXPECTED WAVE FORMS:

Fig 2.2 PCM Waveform with AC Input
WITH DC INPUT:

OBSERVATIONS: PCM Modulation with AC input

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<thead>
<tr>
<th></th>
<th>Amplitude</th>
<th>Time period</th>
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<tbody>
<tr>
<td>AC input</td>
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<tr>
<td>Sample and hold circuit</td>
<td></td>
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<tr>
<td>Clock signal(4KHz)</td>
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<tr>
<td>Clock signal(64KHz)</td>
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<tr>
<td>PCM Output</td>
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<tr>
<td>D/A converter output signal</td>
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<tr>
<td>LPF output signal</td>
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<tr>
<td>Demodulated output</td>
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Fig 2.3 PCM Waveforms/Timing diagram (DC input)
PCM Modulation with DC input

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<tr>
<th></th>
<th>Amplitude</th>
<th>Time period</th>
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<tr>
<td>DC input</td>
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<tr>
<td>Clock signal(4KHz)</td>
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<td></td>
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<tr>
<td>Clock signal(64KHz)</td>
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<tr>
<td>PCM Output</td>
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PCM Demodulated (with DC input)

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<th></th>
<th>Amplitude</th>
<th>Time period</th>
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<tr>
<td>D/A converter output signal</td>
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<tr>
<td>LPF output signal</td>
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<tr>
<td>Demodulated output</td>
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RESULT:
Thus the Pulse Code modulation and demodulation were performed and graphs were plotted.

VIVA QUESTIONS:
1. What do you mean by quantizing process?
2. What will happen when sampling rate is greater than Nyquist rate?
3. What will happen when sampling rate is less than Nyquist rate?
4. Find the A/D Converter output for input DC voltage of 3.6V.
5. Fig shown below shows a PCM wave in which the amplitude levels of +1 volt and -1 volt are used to represent binary symbols 1 and 0 respectively. The code word used consists of three bits. Find the sampled version of an analog signal from which this PCM wave is derived.
6. Mention some applications of PCM.
7. What is the function of Sample and Hold circuit?
EXPERIMENT NO: 02
DPCM MODULATION & DETECTION

AIM:
To analyze a DPCM system and to interpret the modulated and demodulated waveforms for a sampling frequency of 8 KHz.

APPARATUS:
1. DPCM Modulation and Demodulation Trainer Kit
2. Dual Trace oscilloscope
3. Digital Multimeter
4. C.R.O (30MHz)
5. Patch chords.

BLOCK DIAGRAM:

Block diagram of DPCM

THEORY:
Differential PCM is quite similar to ordinary PCM. However, each word in this system indicates the difference in amplitude, positive or negative, between this sample and the previous sample. Thus the relative value of each sample is indicated rather than, the absolute value as in normal PCM. This unique system consists of

I. DPCM Modulator
1. Regulated power supply
2. Audio Frequency signal generator
3. Prediction Filter
4. Sample & Hold circuit
5. A/D Converter
6. Parallel –Serial Shift register
7. Clock generator / Timing circuit
8. DC source

II. DPCM Demodulator
1. Regulated Power Supply
2. Serial-Parallel Shift registers.
3. D/A converter.
4. Clock generator
5. Timing circuit
6. Prediction filter
7. Passive low pass filter

PROCEDURE:
1. Study the theory of operation thoroughly.
2. Connect the trainer (Modulator) to the mains and switch on the power supply.
3. Observe the output of the AF generator using CRO, it should be Sine wave of 400 Hz frequency with 3V pp amplitude.
4. Verify the output of the DC source with multi-meter/scope; output should vary 0 to +290mV.
5. Observe the output of the Clock generator using CRO, they should be 64 KHz and 8 KHz frequency of square with 5 Vpp amplitude.
6. Connect the trainer (De Modulator) to the mains and switch on the power supply.
7. Observe the output of the Clock generator using CRO; it should be 64 KHz square wave with amplitude of 5 pp.

DPCM Operation (with DC input):

Modulation:
8. Keep CRO in dual mode. Connect one channel to 8 KHz signal (one which is connected to the Shift register) and another channel to the DPCM output.
9. Observe the DPCM output with respect to the 8 KHz signal and sketch the waveform.
10. Note: Form this waveform you can observe that the LSB bit enters the output first.
11. Set DC source to some value say 1 V with the help of multi-meter and connect it to the A/D converter input and observe the output LED’s.
12. Note down the digital code i.e. output of the A/D converter and compare with the theoretical value Theoretical value can be obtained by:
\[
\frac{\text{Input voltage}}{1 \text{ LSB Value}} = X_{(10)} = Y_{(2)}
\]

1 LSB value = \( V_{\text{ref}} / 2^n \)

Since \( V_{\text{ref}} = 290\text{mV} \) and \( n= 4 \)

1 LSB Value = 18.125mV

**Demodulation**

1. Connect DPCM signal to the demodulator (S-P register) from the DPCM modulator with the help of coaxial cable (supplied with the trainer).

2. Connect clock signal (64 KHz) from the transmitter to the receiver using coaxial cable.

3. Connect transmitter clock to the timing circuit.

4. Observe and note down the S-P shift register output data and compare it with the transmitted data (i.e. output A/D converter at transmitter) notice that the output of the S-P shift register is following the A/D converter output in the modulator.

5. Observe D/A converter output (demodulated output) using multi-meter/scope and compare it with the original signal and can observe that there is no loss in information in process of conversion and transmission.

**DPCM Operation (with AC input):**

**Modulation:**

6. Connect AC signal of 3VPP amplitude to positive terminal of the summer circuit.

Note: The output of the prediction filter is connected to the negative terminal of the summer circuit and can observe the waveforms at the test points provided on the board.

7. The output of the summer is internally connected to the sample and hold circuit

8. Keep CRO in dual mode. Connect one channel to the AF signal and another channel to the Sample and Hold output. Observe and sketch the sample & hold output

9. Connect the Sample and Hold output to the A/D converter and observe the DPCM output using oscilloscope.

10. Observe DPCM output by varying AF signal voltage.

**Demodulation:**

11. Connect DPCM signal to the demodulator input (S-P shift register) from the DPCM modulator with the help of coaxial cable (supplied with trainer).

12. Connect clock signal (64 KHz) from the transmitter to the receiver using coaxial cable.

13. Connect transmitter clock to the timing circuit.

14. Keep CRO in dual mode. Connect one channel to the sample & hold output and another channel to the D/A converter output.
15. Observe and sketch the D/A output

16. Connect D/A output to the LPF input and observe the output of the LPF.

17. Observe the waveform at the output of the summer circuit.

18. Disconnect clock from transmitter and connect to the local oscillator (i.e., clock generator output from De Modulator) with remaining setup as it is. Observe D/A output and compare it with the previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

**EXPECTED WAVEFORMS:**

Draw the wave forms for the given DC input, corresponding binary data wave form, and for AC input draw sample and hold waveform then D/A converter o/p and then reconstructed AC signal

---

**OBSERVATIONS: DPCM with AC input**

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<thead>
<tr>
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<th>Amplitude</th>
<th>Time period</th>
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<tbody>
<tr>
<td><strong>AC Input</strong></td>
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<td><strong>Prediction Filter Output</strong></td>
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</table>
Sample and Hold Output
Clock -1 output
DPCM Output

Demodulation:

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<tr>
<th></th>
<th>Amplitude</th>
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<tr>
<td>Demodulation Output</td>
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<tr>
<td>Prediction Filter output</td>
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</table>

RESULT:
Thus the Differential Pulse code modulation and demodulation were performed.

VIVA QUESTIONS:
1. For data compression says whether ADPCM or DPCM is better. Justify.
2. What is the need for compression? Mention the types of compression.
3. List the communication standards which use DPCM.
4. Based upon the knowledge that you have gained after doing the experiment write the Functions of sample and hold circuit.
5. Name the circuit used to achieve synchronization between transmitter and receiver.
AIM:
To analyze a Delta modulation system and interpret the modulated and demodulated waveforms

APPARATUS:
1. PCM Modulator trainer- AET-73M
2. PCM Demodulator trainer-AET-73D
3. C.R.O (30MHz)
4. Patch chords.

BLOCK DIAGRAM: DELTA MODULATOR & DEMODULATOR
INTRODUCTION
Delta Modulation is a form of pulse modulation where a sample value is represented as a single bit. This is almost similar to differential PCM, as the transmitted bit is only one per sample just to indicate whether the present sample is larger or smaller than the previous one. The encoding, decoding and quantizing process become extremely simple but this system cannot handle rapidly varying samples. This increases the quantizing noise.

The trainer is a self sustained and well organized kit for the demonstration of delta modulation & demodulation. The system consist of:

DM Modulator (AET-73M) trainer kit
1. Regulated power supply
2. Audio Frequency signal generator
3. Buffer/signal shaping network
4. Voltage comparator
5. 4 Bit UP/DOWN counter
6. Clock generator/Timing circuit
7. 4 Bit D/A converter
8. DC source

DM Demodulator (AET-73D) trainer kit
1. Regulated power supply
2. 4 Bit UP/DOWN counter
3. 4 Bit D/A converter
4. Clock generator
5. Passive low pass filter
6. Audio amplifier

Regulated power supply (73M & 73D):
This consists of a bridge rectifier followed by Capacitor filters and three terminal regulators 7805 and 7905 to provide regulated DC voltages of +5V and +12V@ 300Ma each to the on board circuits. These supplies have been internally connected to the circuits, so no external connections are required for operation.

Audio Frequency (AF) S signal generator (73M):
Sine wave signal of 100 Hz is generated to use as a modulating (message or information) signal to be transmitted. This is an Op-Amp based Wein bridge Oscillators using IC TL084 is a FET.input general purpose Operational Amplifier .Amplitude control is provided in the circuit to vary the output amplitude of AF signal.

Clock generator/Timing circuit (73M & 73D):
A TTL compatible clock signal of 4 KHz frequency is provided on board to use as a clock to the various circuits in the system. This circuit is a astable multivibrator using 555 timer followed by a buffer.

DC Source (73M):
A 0 to +5V variable DC voltage is provided on board to use as a modulating signal instead of AF Signal. is useful to study step by step operation of Delta modulation and Demodulation. This is a simple circuit consists of potentiometer and fixed power supply.

Buffer/Signal shaping circuit (73M):
A non inverting buffer using IC TL 084 is provided at the input of the DM modulator followed by a level shifting network. Buffer provides the isolation between DM circuit and the signal source. Signal Shaping super imposes the 1.5V DC on incoming modulating signal so that the input of the comparator lies between 0 and +3V maximum.

Voltage comparator (73D):
This circuit is build with IC LM339 The LM339 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2mV for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the common mode voltage range includes ground, even though operated from a single power supply voltage. Application areas include limit comparators simple analog to digital converters: pulse, square and time delay generators. wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates .The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic where the low power drain of the LM339 is a distinct advantage over standard comparators .For circuit connections and other operating conditions.

Low pass filters (73D):
This is a series of simple RC networks provided on board to smoothen the output of the D/A converter output. RC values are chosen such that the cutoff frequency would be at 100 Hz.

Amplifiers (73D):
This is an Op-amp (IC TL084) based non-inverting variable gain amplifiers provided on board to amplify the recovered message singles i.e. output of low pass filter to desired level. Amplitude control is provided in circuit to vary the gain of the amplifier between 0 and 6. AC/DC Switch facilitates to couple the input signal through capacitor to directly to the amplifier input.

4 Bit UP/DOWN Counter (73M & 73 D):
This circuit is made using Synchronous 4-Bit Up/Down Counter with Mode Control IC 74LS191. The DM 74LS191 circuit is a synchronous, reversible, counter. Synchronous operation is provided by having all flip-flops clocked simultaneously. So that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with the asynchronous counters. The outputs of the four master slave flip flops are triggered on a LOW to HIGH level transition of the clock input. If the enable input is LOW a HIGH at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is HIGH. The direction of the count is determined by the level of the down/up input. When LOW the counter counts up and when HIGH it counts down. The counter is fully programmable that is the outputs may be preset to either level by placing a LOW on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down/up and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers required for parallel words. The ripple clock input produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high speed operation.

4 Bit D/A converter (AET-73M & 73D):
This has been constructed with a popular 8 bit D/A Converter IC DAC 0808. The DAC0808 is an 8-bit monolithic DAC featuring a full scale output current settling time of 150 Ns while dissipating only 33 maw with +5V supplies. No reference current (I REF) trimming is required for most applications since the full scale output current is typically ḅ- 1 LSB of 255 I REF/256. Relative accuracies of better than + 0.19 % assure 8 bit monotonic and linearity while zero level output current of less than 4 µA provides 8-bit zero accuracy for I REF [ greater than or equal ] 2 math power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. 4 LSB Bits are permanently grounded to make 4 bit converter. For complete specifications and operating conditions please refer the data sheet of DAC0808.

DM Operation:
Figure 4.1 shows the basic block diagram of the PCM system. The modulating signal is applied to buffer /signal shaping network. This applied signal will be superimposed by +1.5V DC so that
the negative portion the modulating signal will clamped to positive ,this process is needed ,because input of the comparator should be between 0 and +3V. After level shifting is done the signal will be passed to inverting input of the comparator. on inverting input of the comparator is connected to output of the 4 Bit D/A converter. Comparator is operating at +5V single supply .So output of the comparator will be high (i.e. +ve Vast) when modulating signal is less than the reference signal i.e. D/A output, otherwise it will be 0V. And this signal is transmitted as DM signal .same signal is also connected as UP/DOWN control to the UP/DOWN counter (74LS 191). UP/DOWN counter is programmed for 0000 starting count. So initially output of the counter is at 0000 and the D/A converter will be at 0V .Comparator compares the modulating signal is greater than the reference signal. For next clock pulse depending on the UP/DOWN input counter will count up or down. If the UP/DOWN input is low (nothing but comparator output). Counter will make up and output will be 0001. So the D/A converter will convert this 0001 digital input to equivalent analog signal(i.e. 0.3V 1 LSB Value).Now the reference signal is 0.3V.If still modulating signal is greater than the D/A output again comparator output(DM) will be low and UP count will occur. If not DOWN Count will take place. This process will continue till the reference signal and modulating signal voltages are equal. So DM signal is a series of 1 and 0. DM signal is applied to a UP/DOWN input of the UP/DOWN counter at the receiver. This UP/DOWN counter is programmed for 1001 initial value (i.e. power on reset) and mode control is activated. So depend on the UP/DOWN input for the next clock pulse counter will count UP or DOWN. This output is applied to 4 Bit D/A converter. A logic circuit is added to the counter which keeps the output of the counter in between 0000 to 1111 always. Output of the D/A converter will be a staircase signal lies between 0 and +4.7V.This staircase signal is applied a low pass filter .This low pass will smoothen the staircase signal so that original AF signal will be recovered. We can use a voltage amplifier at the output of the low pass filter to amplify the recovered AF signal to desired voltage level.

**PROCEDURE:**

**DM Modulator:**
1. Study the theory of operation
2. Connect the trainer (AET-73M) -
3. Observe the output of AF generator using CRO; it should be a Sine wave of 100 Hz frequency with 3Vpp amplitude.
4. Verify the output of the DC source with multimeter/scope; output should vary 0 to +4V
5. Observe the output of the clock generator using Crotchety should be 4 KHz frequency of square wave with 5 Up amplitude.

**Note:** This clock signal is internally connected to the up/down counter so no external connection is required.

**DM With DC Voltage as modulating signal:**
6. Connect DC signal from the DC source to the inverting input of the comparator and set some voltage says 3V.
7. Observe and plot the signals at D/A converter output (i.e. non-inverting input of the comparator), DM signal using CRO and compare them with the waveforms given in figure.
8. Connect DM signal (from 73M) to the DM input of the demodulator.
9. Connect clock (4KHz) from modulator (73M) to the clock input of the demodulator (73D). Connect clock input of UP/DOWN counter (in 73D) to the clock from transmitter with the help of springs provided.
10. Observe digital output (LED indication) of the UP/DOWN counter (in 73D) and compare it with the output of the UP/DOWN (in 73M). By this you can notice that the both the outputs are same.
11. Observe and plot the output of the D/A converter and compare it with the waveforms given in figure.
12. Measure the demodulated signal (i.e. output of the D/A converter 73D with the help of multimeter and compare it with the original signal 73 M. From the above observation you can notice that both the voltages are equal and there is no loss in process of modulation, transmission and demodulation.
13. Similarly you can verify the DM operation for different values of modulating signal.

**DM With AF Voltage as modulating signal:**
14. Connect AF signal from the AF source to the inverting input of the comparator and set some voltage says 3V.
15. Observe and plot the signals at D/A converter output (i.e. non-inverting input of the comparator), DM signal using CRO and compare them with the waveforms given in figure.
16. Connect DM signal (from 73M) to the DM input of the demodulator.
17. Connect clock (4KHz) from modulator (73M) to the clock input of the demodulator (73D).
18. Connect clock input of UP/DOWN counter (in 73D) to the clock from transmitter with the help of springs provided.
19. Observe and plot the output of the D/A converter and compare it with the waveforms given in figure.
20. Observe and sketch the D/A output.
21. Connect D/A output to the LPF input.
22. Observe the output of the LPF/Amplifier and compare it with the original modulating signal (AET-73M).
23. From the above observation you can verify that there is no loss in information in conversion and transmission process.
24. Disconnect clock from transmitter (AET-73M) and connect to local oscillator (i.e. clock generator output from AET-73D) with remaining setup as it is. Observe demodulated signal output and compare it with the previous result. This signal is little bit distorted in shape. This is because lack of synchronization between clock at transmitter and clock at receiver.

**Note:** you can take modulating signals from external sources. Maximum amplitude should not exceed 4 V in case of DC and 3 Vpp in case of AC (AF) signals.
EXPECTED WAVE FORMS: FOR AC INPUT
FOR DC INPUT
OBSERVATIONS: DM MODULATION WITH AC INPUT

<table>
<thead>
<tr>
<th></th>
<th>amplitude</th>
<th>Time period</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC input</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D/A converter output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock signal (4 KHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DM output</td>
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<td></td>
</tr>
</tbody>
</table>

DM DEMODULATION WITH AC INPUT
### DM MODULATION WITH DC INPUT

<table>
<thead>
<tr>
<th>Source</th>
<th>Amplitude</th>
<th>Time Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>DM input</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D/A converter output signal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Demodulated Output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock signal (4 KHz)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### DM DEMODULATION WITH DC INPUT

<table>
<thead>
<tr>
<th>Source</th>
<th>Amplitude</th>
<th>Time Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>DM input</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D/A converter output signal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Demodulated Output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock signal (4 KHz)</td>
<td></td>
<td></td>
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</tbody>
</table>

**RESULT:**
Thus the Delta modulation and demodulation were performed and graphs were plotted.

**VIVA QUESTIONS:**
1. Compare DPCM, PCM & Delta modulation.
2. How to reduce the quantization noise that occurs in DM?
3. A band pass signal has a spectral range that extends from 20 to 82 KHz. Find the acceptable sampling frequency.
4. Find the Fourier series expansion of an Impulse train.
5. Mention the applications of DM.
TIME DIVISION MULTIPLEXING SYSTEM

AIM: Study of Time Division Multiplexing System.

APPARATUS USED:
1. TDM Trainer Kit
2. C.R.O
3. Connecting leads

THEORY:

An important feature of pulse-amplitude modulation is a conservation of time. That is, for a given message signal, transmission of the associated PAM wave engages the communication channel for only a fraction of the sampling interval on a periodic basis. Hence, some of the time interval between adjacent pulses of the PAM wave is cleared for use by the other independent message signals on a time-shared basis. By so doing, we obtain a time-division multiplex system (TDM), which enables the joint utilization of a common channel by a plurality of independent message signals without mutual interference. Each input message signal is first restricted in bandwidth by a low-pass pre-alias filter to remove the frequencies that are nonessential to an adequate signal representation.

BLOCK DIAGRAM:

PROCEDURE:
MULTIPLEXER:
1. Observe the AF generator-1 output and note down the amplifier and frequency.
2. Observe the AF generator-2 output and note down the amplitude and frequency.

3. Observe the AF generator-2 output and note down the amplitude and frequency.

4. Connect the AF generator 1, 2 and 3 outputs to CH1, CH2 & CH3 of TDM multiplexer.

5. Observe and connect the clock generator output to the control input of the TDM multiplexer (it acts like selection line for MUX).

6. Observe the TDM output in storage oscilloscope.

**DEMULTIPLEXER:**

6. Using coaxial cable connect the TDM de-multiplexer.

7. Connect the clock generator output in de-multiplexer trainer to the control input of the TDM de-multiplexer.

8. Observe the de-multiplexed signals at CH1, CH2 and CH3.

9. Connected the CH1, CH2 and CH3 outputs to low pass filter and amplifier and note down the outputs.

**WAVEFORMS:**
1.8. OBSERVATION

<table>
<thead>
<tr>
<th>Transmitter Section</th>
<th>Receiver Section</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Signal 1</strong></td>
<td><strong>Demultiplexed Signal 1</strong></td>
</tr>
<tr>
<td>Amplitude</td>
<td>Time Period</td>
</tr>
<tr>
<td><strong>Signal 2</strong></td>
<td><strong>Demultiplexed Signal 2</strong></td>
</tr>
<tr>
<td>Amplitude</td>
<td>Time Period</td>
</tr>
<tr>
<td><strong>Transmitter Output</strong></td>
<td><strong>Filtered Demultiplexed Signal 1</strong></td>
</tr>
<tr>
<td>Amplitude</td>
<td>Time Period</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Amplitude</td>
<td>Time Period</td>
</tr>
</tbody>
</table>

**RESULT:** Time Division Multiplexing System signal has been verified & observed successfully.

1. What is meant by multiplexing technique and what are the different types of Multiplexers?
2. Briefly explain about TDM & FDM?
3. What is the transmission bandwidth of a PAM/TDM signal?
4. Define crosstalk effect in PAM/TDM system?
5. What are the advantages of TDM system?
6. What are major differences between TDM & FDM?
7. Give the value of Ts in TDM system?
8. What are the applications of TDM system and give some example?
9. What is meant by signal overlapping?
10. Which type of modulation technique will be used in TDM?
FSK - GENERATION AND DETECTION

**AIM:**
To analyze a FSK modulation system. And interpret the modulated and demodulated waveforms

**APPARATUS:**
1. FSK Trainer Kit - AET-48
2. Dual Trace oscilloscope
3. Digital Multimeter
4. C.R.O (30MHz)
5. Patch chords.

**BLOCK DIAGRAM:**

![Block Diagram](image)

**THEORY:**
In Frequency shift keying, the carrier frequency is shifted (i.e. from one frequency to another) corresponding to the digital modulating signal. If the higher frequency is used to represent a data ‘1’ & lower frequency a data ‘0’, the resulting FSK waveform appears.
Thus
Data =1 High Frequency
Data =0 Low Frequency

It is also represented as a sum of two ASK signals. The two carriers have different frequencies & the digital data is inverted. The demodulation of FSK can be carried out by a PLL. As known,
the PLL tries to ‘lock’ the input frequency. It achieves this by generating corresponding O/P voltage to be fed to the VCO, if any frequency deviation at its I/P is encountered. Thus the PLL detector follows the frequency changes and generates proportional O/P voltage. The O/P voltage from PLL contains the carrier components. Therefore to remove this, the signal is passed through Low Pass Filter. The resulting wave is too rounded to be used for digital data processing. Also, the amplitude level may be very low due to channel attenuation.

**FSK Modulator**
The FSK modulator using IC XR 2206. IC XR 2206 is a VCO based monolithic function generator capable of producing Sine, Square, Triangle signals with AM and FM facility. In this trainer XR2206 is used generate FSK signal. Mark (Logic 1) and space (logic 0) frequencies can be independently adjusted by the choice of timing potentiometers FO & FI. The output is phase continuous during transitions. The keying signals i.e. data signal is applied to pin 9.

**FSK Demodulator:**
FSK demodulator in a combination of PLL (LM565) and comparator (Op-amp). The frequency-changing signal at the input to the PLL drives the phase detector to result in rapid change in the error voltage, which is applied to the input of the comparator. At the space frequency, the error voltage out of the phase detector is below the comparison voltage of the comparator. The comparator is a non-inverting circuit, so its output level is also low. As the phase detector input frequency shifts low (to the mark frequency), the error voltage steps to a high level, passing through the comparison level, causing the comparator output voltage to go high. This error voltage change will snap the comparator output voltage between its two output levels in manner that duplicates the data signal input to the XR22OS modulator. The free running frequency of the PLL (no input signal) is set midway between the mark and space frequencies. A space at 2025 Hz and mark at 2225 Hz will have a free running VCO frequency of 2125 Hz.

**5.6 TEST PROCEDURE**
1. Connect the trainer kit to the mains and switch on the power supply
2. Check internal RPS voltage (it should be 12V) and logic source voltage for logic one (it should be 12V)
3. Observe the data signal using oscilloscope. Note down the value. (Amplitude and Time Period)
4. Connect the output of the logic source to data input of the FSK modulator
5. Set the output frequency of the FSK modulator as 1.2 KHz using control F0 (this represents logic 0). Then set another frequency as 2.4 KHz using control F1 (this represents logic 1) using multimeter.
6. Connect the data input of the FSK modulator to the output of the data signal generator. Observe the signal that comes out of FSK modulator and note down the readings.
7. Connect the FSK modulator output to the input of the FSK demodulator. Observe the waveform of FSK demodulator output using CRO and note down the readings
**OBSERVATIONS:**

<table>
<thead>
<tr>
<th>Data source</th>
<th>Carrier signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Type</td>
<td>Time Period</td>
</tr>
<tr>
<td>Square Wave</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
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</tbody>
</table>

**Modulated Output**

<table>
<thead>
<tr>
<th>Modulated Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal name</td>
</tr>
<tr>
<td>FSK</td>
</tr>
</tbody>
</table>

**Demodulated Output**

<table>
<thead>
<tr>
<th>Demodulated Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Type</td>
</tr>
<tr>
<td>Square Wave</td>
</tr>
</tbody>
</table>

**EXPECTED WAVE FORMS:**

![Waveforms Diagram](image-url)
RESULT:
The FSK modulation and demodulation were performed and required graphs were plotted.

VIVA QUATIONS:
1. What is MSK?
2. For the given 8 bit data 10111010 draw the FSK output waveform.
3. Draw the constellation diagram of FSK.
4. What will happen if the same frequency is used for both the carriers?
**AIM:**
To analyze a PSK modulation system. And interpret the modulated and demodulated waveforms.

**APPARATUS:**
1. BPSK Trainer Kit - AET-48
2. Dual Trace oscilloscope
3. Digital Multimeter
4. C.R.O (30MHz)
5. Patch chords.

**BLOCK DIAGRAM:**

**Theory:**
Phase shift keying is a modulation/data transmitting technique in which phase of the carrier signal is shifted between two distinct levels. In a simple PSK (ie binary PSK) unshifted carrier $V\cos\omega_0t$ is transmitted to indicate a 1 condition, and the carrier shifted by 180° ie $-V\cos\omega_0t$ is transmitted to indicate as 0 condition.

**PSK Modulator**
Figure 6.2 shows the PSK modulator. IC CD 4052 is a 4 channel analog multiplexer and is used as an active component in this circuit. One of the control signals of 4052 is grounded so that 4052 will act as a two channel multiplexer and other control is being connected to the binary signal ie data to be transmitted. Unshifted carrier signal is connected directly to CH1 and carrier shifted by 180° is connected to CH2. phase shift network is a unity gain inverting amplifier using OP-amp (TL084).
When input data signal is 1 i.e. control signal is at high voltage, output of the 4052 is connected to CH1 and unshifted (or 0 phase) carrier is passed on to output. Similarly When data signal is 0 i.e. control signal is at zero voltage output of 4052 is connected to CH2 and carrier shifted by 1800 is passed on to output.

**PSK Demodulator:**
Demodulation of PSK is achieved by subtracting the received carrier from a derived synchronous reference carrier of constant phase. Figure shows the simple coherent(synchronous) PSK modulator. Received PSK signal is converted to square wave using an op-amp(TL084) based zero crossing detector and connected to EX-OR circuit. The derived reference carrier is connected to other input of the EX-OR Gate through an op-amp based zero crossing detector. For the simplicity same carrier is used at receiver as reference carrier (In practical communication system reference carrier is generated at receiver). We can observe the exact operation of demodulator with the help of waveforms at various nodes in the circuit. Received PSK signal is converted to square wave using an op-amp(TL084) based zero crossing detector and connected to EX-OR circuit. The derived reference carrier is connected to other input of the EX-OR Gate through an op-amp based zero crossing detector. For the simplicity same carrier is used at receiver as reference carrier (In practical communication system reference carrier is generated at receiver). We can observe the exact operation of demodulator with the help of waveforms at various nodes in the circuit.

**PROCEDURE:**

6.6 **PROCEDURE**
1. Connect the trainer to mains and switch on the power supply.
2. Measure the output of the regulated power supply ie +5V and -5V with the help of digital multimeter.
3. Observe the output of the carrier generator using CRO, it should be an 8KHZ sine with 5Vpp amplitude.
4. Observe the various data signals(1KHZ,2KHZ and 4KHZ0 using CRO)

6.6.1 **Modulation:**
5. Connect carrier signal to carrier input of the PSK modulator.
6. Connect data signal say 4KHZ from data source to data input of the modulator.
7. Keep CRO in dual mode and connect CH1 input of the CRO to data signal and CH2 to the output of the PSK modulator.
8. Observe the PSK output signal with respect to data signal and plot the waveforms.
6.6.2 Demodulation:
9. Connect the PSK output to the PSK input of the demodulator.
10. Connect carrier to the carrier input of the PSK demodulator.
11. Keep CRO in dual mode and connect CH1 to data signal (at modulator) and CH2 to the output of the demodulator.
12. Compare the demodulated signal with the original signal. By this we can notice that there is no loss in modulation and demodulation process.
13. Repeat the steps 6 to 12 with different data signals ie 2KHZ and 1KHZ

EXPECTED GRAPHS:
OBSERVATIONS: PSK MODULATION

<table>
<thead>
<tr>
<th>Carrier signal</th>
<th>Amplitude</th>
<th>Time period</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Source</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For 4KHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>For 2KHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>For 1KHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Modulated Output</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For 4KHz</td>
<td></td>
<td></td>
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<tr>
<td>For 2KHz</td>
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<td></td>
</tr>
<tr>
<td>For 1KHz</td>
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</table>

PSK DEMODULATION

<table>
<thead>
<tr>
<th>Demodulated Output</th>
<th>Amplitude</th>
<th>Time period</th>
</tr>
</thead>
<tbody>
<tr>
<td>For 4KHz</td>
<td></td>
<td></td>
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<tr>
<td>For 2KHz</td>
<td></td>
<td></td>
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<tr>
<td>For 1KHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

RESULT:
Thus the PSK modulation and demodulation were performed and graphs were plotted.

VIVA QUESTIONS:
1. Compare FSK and PSK.
2. List the Characteristics of TL084 op-amp.
3. Compare TL084 op amp with IC 741 op amp.
4. What do we infer from constellation diagrams of various modulation schemes?
AIM: To study the process of ASK modulation and demodulation and study various data formatting modulation and demodulation techniques.

APPARATUS: 1. ASK MODULATION & DEMODULATION Trainer.
            2. CRO 30MHz Dual Channel.
            3. Patch Chords.

THEORY:-

Modulation also allows different data streams to be transmitted over the same channel. This process is called as ‘Multiplexing’ & result in a considerable saving in bandwidth no of channels to be used. Also it increases the channel efficiency. The variation of particular parameter variation of the carrier wave gives rise to various modulation techniques. Some of the basic modulation techniques are described as under. ASK:- In this modulation involves the variation of the amplitude of the carrier waves in accordance with the data stream. The simplest method of modulating a carrier with a data stream is to change the amplitude of the carrier wave every time the data changes. This modulation technique is known as amplitude shift keying. The simplest way of achieving amplitude shift keying is ‘ON’ the carrier whenever the data bit is ‘HIGH’ & switching ‘OFF’ when the data bit is low i.e. the transmitter outputs the carrier for HIGH & totally suppresses the carrier for low. This technique is known as ON-OFF keying. Fig. illustrates the amplitude shift keying for the given data stream. Thus, DATA = HIGH CARRIER TRANSMITTED DATA = LOW CARRIER SUPPRESSED

The ASK waveform is generated by a balanced modulator circuit, also known as a linear multiplier, As the name suggests, the device multiplies the instantaneous signal at its two inputs, the output voltage being product of the two input voltages at any instance of time. One of the inputs is a/c coupled ‘carrier’ wave of high frequency. Generally the carrier wave is a sine wave since any other waveform would increase the bandwidth imparting any advantages requirement without improving or to it. The other i/p which is the information signal to be transmitted, is D.C. coupled. It is known as modulating signal

In order to generate ASK waveform it is necessary to apply a sine wave at carrier input & the digital stream at modulation input. The double balanced modulator is shown in fig.
The data stream applied is unipolar i.e. 0Volt at logic LOW & +4.5Volts at logic HIGH. The output of balanced modulator is a sine wave, unchanged in phase when a data bit ‘HIGH’ is applied to it. In this case the carrier is multiplied with a positive constant voltage when the data bit LOW is applied, the carrier is multiplied by 0 Volts, giving rise to 0Volt signal at modulator’s o/p. The ASK modulation results in a great simplicity at the receiver. The method to demodulate the ASK waveform is to rectify it, pass it through the filter &’square up’ the resulting waveform. The o/p is the original digital data stream. Fig. shows the functional blocks required in order to demodulate the ASK waveform at receiver

**PROCEDURE:**

**Modulation:**

1. Connect the sine wave 500 KHz from the carrier generator TP1 to the carrier input of the modulator TP7.

2. And also connect data clock D1 i.e., modulation signal TP3 to the modulation input TP8. 3. Switch ON the power supply.

4. Observe the output at TP9.

5. By varying the gain pot P3 observe the ASK output at TP10.

6. Adjusting the carrier offset and modulation offset we can observe the ASK output.

7. By changing the carrier signal 1MHz and different data clocks D2, D3, D4 observe the output.
Demodulation:-

1. Connect ASK output TP10 to the rectifier input TP12 and observe the waveform.

2. Now connect rectifier output TP13 to the low pass filter input TP14 and observe the output at TP15.

3. CONNECT LPF output TP15 to the data squaring circuit input TP16 and observes the demodulation output waveform at TP17.

4. By changing the different data clocks and observe the demodulation output.

**EXPECTED WAVEFORMS:**
RESULT: Thus the ASK modulation and demodulation were performed and graphs were Plotted.

VIVA QUESTIONS:
1. Compare ASK and PSK.
2. List the advantages of ASK.
3. Applications of ASK.
EXPERIMENT NO: 09
DPSK GENERATION & DETECTION

**AIM:** Study the characteristics of differential phase shift keying

**APPARATUS:**
1. DPSK Trainer Kit
2. Dual Trace oscilloscope
3. Digital Multimeter
4. C.R.O (30MHz)
5. Patch chords.

**BLOCK DIAGRAM:**
**THEORY:**

DPSK: Phase Shift Keying requires a local oscillator at the receiver which is accurately synchronized in phase with the un-modulated transmitted carrier, and in practice this can be difficult to achieve. Differential Phase Shift Keying (DPSK) overcomes the difficult by combining two basic operations at the transmitter (1) differential encoding of the input binary wave and (2) phase shift keying – hence the name differential phase shift keying. In other words DPSK is a non-coherent version of the PSK.

The differential encoding operation performed by the modulator is explained below. Let b(t) be the binary message to be transmitted. An encoded message stream b(t) is generated from b'(t) by using a logic circuit. The first bit in b(t) is arbitrary which may be chosen as 1 or 0. The subsequent bits in b(t) are determined on the basis of the rule that when b'(t) is 1 b(t) does not change its value. In the first bit stream, the initial bit (arbitrary) is 1 and in the second bit stream, the initial bit is 0. EX-NOR gate can be used to perform this operation as its output is a 1 when both the input are same, and a 0 when the inputs are different.

<table>
<thead>
<tr>
<th>b'(t)</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>b(t)</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Phase</td>
<td>0°</td>
<td>180°</td>
<td>180°</td>
<td>180°</td>
<td>0°</td>
</tr>
<tr>
<td>B(t)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Phase</td>
<td>180°, 0°</td>
<td>0°</td>
<td>0°</td>
<td>180°</td>
<td>0°</td>
</tr>
</tbody>
</table>
Example for Complete DPSK operation (with arbitrary bit as 0):

Message signal (to be transmitted) 0 1 1 0 0
Encoded data (differential data) 0 1 1 1 0
Transmitted signal phase: 180° 0° 0° 0° 180° 0°
Received signal phase: 180° 0° 0° 0° 180° 0°
Encoded data (differential data) 0 1 1 1 0
Message signal (Demodulation) 0 1 1 0 0

DPSK Modulator: IC CD 4052 is a 4 channel analog multiplexer and is used as an active component in this circuit. One of the control signals of 4052 is grounded so that 4052 will act as a two channel multiplexer and other control is being connected to the binary signal i.e., encoded data. Un- shifted carrier signal is connected directly to CH1 and carrier shifted by 1800is connected to CH2. Phase shift network is a unity gain inverting amplifier using Op-Amp (TL084).

When control signal is at high voltage, output of the 4052 is connected to CH1 and un-shifted (or 0 phase) carrier is passed on to output. Similarly when control signal is at zero voltage output of 4052 is connected to CH2 and carrier shifted by 1800 is passed on to output.

Differential encoder: This consists of 1 bit delay circuit and an X-NOR Gate. 1 bit delay circuit is formed by a D-Latch. Data signal i.e., signal to be transmitted is connected to one of the input of the X-NOR gate and other one being connected to out of the delay circuit. Output of the X-NOR gate and is connected to control input of the multiplexer (IC 4052) and as well as to input of the D-Latch. Output of the X-NOR gate is 1 when both the inputs are same and it is 0 when both the inputs are different.

DPSK Demodulator: This consists of 1 bit delay circuit, X-NOR Gate and a signal shaping circuit. Signal shaping circuit consists of Op-amp based zero crossing detector followed by a D-latch. Receiver DPSK signal is converted to square wave with the help of zero crossing and this square wave will pass through the D-Latch. So output of the D-latch is an encoded data. This encoded data is applied to 1 bit delay circuit as well as to one of the inputs of X-NOR gate. And output of the delay circuit is connected to another input of the X-NOR gate. Output of the X-NOR gate is 1 when both the inputs are same and it is 0 when both the inputs are different.

PROCEDURE: MODULATOR

1. Connect carrier signal to carrier input of the PSK Modulator.
2. Connect data signal from data input of the X-NOR gate.
3. Keep CRO in dual mode.
4. Connect CH1 input of the CRO to data signal and CH2 input to the encoded data (which is nothing but the output of the X-NOR gate)
5. Observe the encoded data with respect to data input. The encoded data will be in a given sequence.

6. Actual data signal: 10101101001010110100

7. Encoded data signal: 01100011011001110010

8. Now connect CH2 input of the CRO to the DPSK output and CH1 input to the encoded data. Observe the input and output waveforms and plot the same.

9. Compare the plotted waveforms with the given waveforms in fig: 1.3

10. Note: Observe and plot the waveforms after perfect triggering. Better to keep the encoded data more than 4 cycles for perfect triggering.

**DEMODULATOR**

1. Connect DPSK signal to the input of the signal shaping circuit from DPSK transmitter with the help of coaxial cable (supplied with trainer).

2. Connect clock from the transmitter (i.e. DPSK Modulator) to clock input of the 1 bit delay circuit using coaxial cable.

3. Keep CRO in dual mode. Connect CH1 input to the encoded data (at modulator) and CH2 input to the encoded data (at demodulator).

4. Observe and plot both the waveforms and compare it with the given waveforms. You will notice that both the signals are same with one bit delay.

5. Keep CRO in dual mode. Connect CH1 input to the data signal (at modulator) and CH2 input to the output of the demodulator.

6. Observe and plot both the waveforms and compare it with the given waveforms. You will notice that both the signals are same with one bit delay.

7. Disconnect clock from transmitter and connect to local oscillator clock (i.e., clock generator output from De Modulator) with remaining setup as it is. Observe demodulator output and compare it with the previous output. This signal is little bit distorted. This is because lack of synchronization between clock at modulator and clock at demodulator. You can get further perfection in output waveform by adjusting the locally generated clock frequency by varying potentiometer.
EXPECTED WAVEFORMS:

RESULT:
Thus the DPSK modulation and demodulation were performed and graphs were plotted.

VIVA QUESTIONS:
1. Define DPSK?
2. Mention the Advantages of DPSK?
3. Mention the Disadvantages of DPSK?
4. Draw the waveforms of DPSK?
5. Compare ASK, PSK, FSK & DPSK?
6. What are the Applications of DPSK?
AIM: To study modulation and demodulation of QPSK and sketch the relevant waveforms.

APPARATUS:
1. QPSK Trainer Kit
2. Dual Trace oscilloscope
3. Digital Multimeter
4. C.R.O (30MHz)
5. Patch chords.

BLOCK DIAGRAM: QPSK MODULATOR & DEMODULATOR

Fig: QPSK Modulator
### THEORY:

**Quadrature Phase Shift Keying**

Phase of the carrier takes on one of four equally spaced values such as $\pi/4$, $3\pi/4$, $5\pi/4$, $7\pi/4$.

$$S_i(t) = \sqrt{2E/T_b} \cos \{2\pi f_c t + (2i - 1)\pi/4\}, \quad 0 \leq t \leq T_b$$

0, elsewhere

Where $i = 1, 2, 3, 4$, & $E = \text{Tx signal energy per symbol}$

$T_b = \text{symbol duration}$

Each of the possible value of phase corresponds to a pair of bits called dibits.

Thus the gray encoded set of dibits: 10,00,01,11

$$S_i(t) = \sqrt{2E/T_b} \cos [(2i - 1)\pi/4] \cos (2\pi f_c t) - \sqrt{2E/T_b} \sin [(2i - 1)\pi/4]$$

$$\sin (2\pi f_c t), \quad 0 \leq t \leq T_b \quad 0, \quad \text{else where}$$

There are two orthonormal basis functions

$$\phi_1(t) = \sqrt{2}/T_b \cos 2\pi f_c t, \quad 0 \leq t \leq T_b$$

$$\phi_2(t) = \sqrt{2}/T_b \sin 2\pi f_c t, \quad 0 \leq t \leq T_b$$

The i/p binary sequence $b(t)$ is represented in polar from with symbols 1 & 0 represented as $+\sqrt{E}/2$ and $-\sqrt{E}/2$. This binary wave is demultiplexed into two separate binary waves consisting of odd & even numbered I/P bits denoted by $b_1(t)$ & $b_2(t)$

$b_1(t)$ & $b_2(t)$ are used to modulate a pair of quadrature carrier or orthogonal Basis function $\phi_1(t)$ & $\phi_2(t)$. The result is two PSK waves. These two binary PSK waves are added to produce the desired QPSK signal.
**PROCEDURE:**

1. Connect and switch on the power supply.
2. QPSK is selected by default and LEDs of corresponding technique will glow.
3. Select the bit pattern using push button i.e. 8 bit or 16 bit or 32 bit or 64 bit. Observe bit pattern on TP-2.
4. Select data rate using push button i.e. 2 KHz or 4 KHz or 8 KHz 16 KHz.

**Modulation:**
5. Observe the input bit pattern at TP-2 by varying bit pattern using respective push button.
6. Observe the data rate at TP-1 by varying data rate using respective push button.
7. Observe the Two-bit encoding i.e. I-Channel (TP-3) and Q-Channel (TP-4).
8. Observe carrier signal i.e. cosine wave (TP-5) and sine wave (TP-6). Frequency of carrier signal will change with respect to data rate.
9. Observe I-Channel (TP-7) and Q-Channel (TP-8) modulated signal.
10. **Observe QPSK modulated signal at TP-9.**

**Demodulation:**
11. Apply the QPSK modulated output to the demodulator input.
12. Observe the multiplied signal of QPSK and carrier signal, cosine at TP-12 and also observe the multiplied signal of QPSK and carrier signal, sine at TP-13.
13. Observe the integrated output at I-channel (TP-14) and Q-channel (TP-15).

### Input Bits | Phase of QPSK signal | Co-ordinates of message signal |
<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>10</td>
<td>π/4</td>
<td>$\sqrt{E/2}$</td>
</tr>
<tr>
<td>00</td>
<td>3π/4</td>
<td>$−\sqrt{E/2}$</td>
</tr>
<tr>
<td>01</td>
<td>5π/4</td>
<td>$−\sqrt{E/2}$</td>
</tr>
<tr>
<td>11</td>
<td>7π/4</td>
<td>$+\sqrt{E/2}$</td>
</tr>
</tbody>
</table>
EXPECTED WAVE FORMS:

RESULT: QPSK modulation and demodulation wave forms are observed.

VIVA QUESTIONS:

11.8 POST LAB QUESTIONS
1. Draw the constellation diagram of QPSK.
2. Give some applications of QPSK modulation scheme
3. Find the output of the following command.
   \[ 5^{(2/3)} - 25 / (2*3) \]
4. What is the relationship between 4 QAM and QPSK?
5. Design a SIMULINK model for QPSK.
AIM: To study the operation of pulse width modulation and to plot spectrum of PAM and PWM.

EQUIPMENT:
1. PWM demonstrator trainer.
2. Dual trace oscilloscope (Storage oscilloscope is desirable).
3. Digital multimeter.
4. Patch cords.

BLOCK DIAGRAM:

PROCEDURE:
Observation of PWM with AC input signal:
1. Study the circuit operation thoroughly.
2. Switch on the trainer and measure the output voltages of the regulated power supply i.e. +5V and -5V.
3. Observe the output of the AF generator using CRO, note that the output is 5V p-p @ 400 Hz frequency.
4. Observe the output of the control signal generator i.e. ramp and reference pulse using CRO.
5. Now connect AF signal to the modulator and observe output waveform (condition: scope is in dual mode, CH 1 is connected to AF signal and CH 2 is connected to PWM output, trigger source in CH 1, if you are using storage oscilloscope after setting AF input voltage observe output in stop mode).

**Procedure to obtain Spectrum:**
6. Observe the output of PWM with the help of Spectrum analyzer and note down the frequencies of harmonics.
7. Draw the spectrum.

**SPECTRUM OF PWM**
RESULT: spectrum of PAM and PWM is observed.